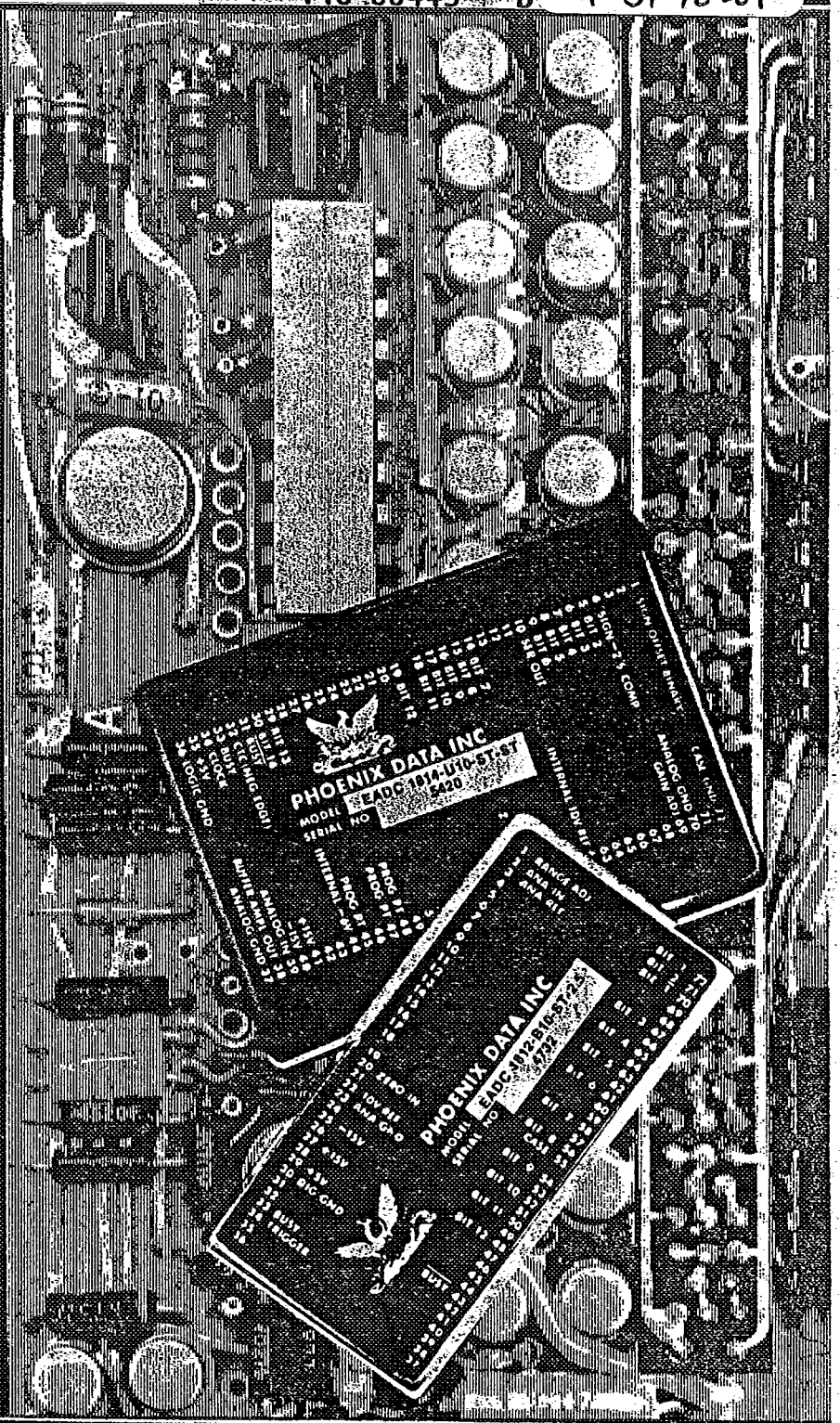
Series 1300 thru 1800 ENCASED ANALOG TO DIGITAL CONVERTERS

A/D Converters for precision and reliability

Features

- 6 Series, 42 Different Models
- 8 to 14 Bit Resolution
- Temperature Compensation to 2.5ppm/°C
- Conversion Times to 2μSec for 8 Bits, 4μSec for 12 Bits and 12μSec for 14 Bits.
- Accuracy to 0.01% of FSR
- Optional Temperature Ranges From -55°C to +90°C
- Programmable Input Range Selection
- Bipolar or Unipolar Input
- Precision Internal Voltage Reference
- Pre-Calibrated for Specified Temperature Range
- RFI and EMI Shielded
- Guaranteed Monotonicity
- Convenient Printed Circuit Board Mounting



General Description

Phoenix Data precision Analog to Digital Converters set the pace for modern industrial, commercial and military applications — providing a wide range of cost and performance configurations to meet the needs of your most demanding specification. Time-proven reliability, ease of application and inherent stability have made Phoenix Data converters the leading choice of designers the world over.

Phoenix Data's Series 1300 thru 1800 Analog to Digital Converters employ the latest in precision components and design technology — using the highly reliable voltage switching, successive approximation conversion technique. Each converter is totally self-contained except for external power requirements of ±15 and 5 volts DC. All units are factory calibrated to published specifications for the specified input and temperature range, with no further adjustment required to maintain specified accuracy and monotonicity.

Each converter consists of an analog input comparator with optional input buffer amplifier for 13 and 14 bit models, a TTL compatible successive approximation register, level shifters and solid-state analog switches, precision ladder network and a temperature compensated internal voltage reference generator — and each converter is totally repairable. The dual-in-line pinout configuration (0.100 inch grid centers) allows convenient printed circuit board mounting.

PDI

Phoenix Data, Inc.

Series 1300 thru 1800
ENCASED ANALOG TO DIGITAL CONVERTERS
A/D Converters for precision and reliability

Series 1300 (10.0KHz to 66.6KHz)

Model	Conversion Time (Note 1)	Accuracy of FSR (±) (Note 2)	Linearity of FSR (±)	Input Impedance	Temperature Coefficient (0°C to 70°C) Note 3	Output Resolution
1308	15 µSec	0.400%	0.200%	20 Kohms	15 ppm/°C	8 Bits
1309	20 µSec	0.200%	0.100%	20 Kohms	15 ppm/°C	9 Bits
1310	25 µSec	0.100%	0.050%	20 Kohms	15 ppm/°C	10 Bits
1311	30 µSec	0.050%	0.025%	20 Kohms	15 ppm/°C	11 Bits
1312	40 µSec	0.025%	0.013%	20 Kohms	15 ppm/°C	12 Bits
1313	50 µSec	0.015%	0.010%	20 Kohms	10 ppm/°C	13 Bits
1314	100 µSec	0.010%	0.005%	20 Kohms	10 ppm/°C	14 Bits

Series 1400 (14.3KHz to 83.3KHz)

1408	12 µSec	0.400%	0.200%	20 Kohms	15 ppm/°C	8 Bits
1409	14 µSec	0.200%	0.100%	20 Kohms	15 ppm/°C	9 Bits
1410	17 µSec	0.100%	0.050%	20 Kohms	15 ppm/°C	10 Bits
1411	20 µSec	0.050%	0.025%	20 Kohms	15 ppm/°C	11 Bits
1412	24 µSec	0.025%	0.013%	20 Kohms	15 ppm/°C	12 Bits
1413	35 µSec	0.015%	0.010%	20 Kohms	10 ppm/°C	13 Bits
1414	70 µSec	0.010%	0.005%	20 Kohms	10 ppm/°C	14 Bits

Series 1500 (28.6KHz to 125KHz)

1508	8 µSec	0.400%	0.200%	20 Kohms	10 ppm/°C	8 Bits
1509	9 µSec	0.200%	0.100%	20 Kohms	10 ppm/°C	9 Bits
1510	10 µSec	0.100%	0.050%	20 Kohms	10 ppm/°C	10 Bits
1511	12 µSec	0.050%	0.025%	20 Kohms	10 ppm/°C	11 Bits
1512	15 µSec	0.025%	0.013%	20 Kohms	10 ppm/°C	12 Bits
1513	25 µSec	0.015%	0.010%	4 Kohms	5 ppm/°C	13 Bits
1514	35 µSec	0.010%	0.005%	4 Kohms	5 ppm/°C	14 Bits

Series 1600 (50KHz to 166.6KHz)

1608	6 µSec	0.400%	0.200%	20 Kohms	10 ppm/°C	8 Bits
1609	7 µSec	0.200%	0.100%	20 Kohms	10 ppm/°C	9 Bits
1610	8 µSec	0.100%	0.050%	20 Kohms	10 ppm/°C	10 Bits
1611	9 µSec	0.050%	0.025%	20 Kohms	10 ppm/°C	11 Bits
1612	10 µSec	0.025%	0.013%	20 Kohms	10 ppm/°C	12 Bits
1613	15 µSec	0.015%	0.010%	4 Kohms	5 ppm/°C	13 Bits
1614	20 µSec	0.010%	0.005%	4 Kohms	5 ppm/°C	14 Bits

Series 1700 (66.6KHz to 285.7KHz)

1708	3.5 µSec	0.400%	0.200%	20 Kohms	10 ppm/°C	8 Bits
1709	4.0 µSec	0.200%	0.100%	20 Kohms	10 ppm/°C	9 Bits
1710	4.5 µSec	0.100%	0.050%	20 Kohms	10 ppm/°C	10 Bits
1711	5.0 µSec	0.050%	0.025%	20 Kohms	10 ppm/°C	11 Bits
1712	6.5 µSec	0.025%	0.013%	20 Kohms	10 ppm/°C	12 Bits
1713	10.0 µSec	0.015%	0.010%	4 Kohms	5 ppm/°C	13 Bits
1714	15.0 µSec	0.010%	0.005%	4 Kohms	5 ppm/°C	14 Bits

Series 1800 (100KHz to 500KHz)

1808	2.0 µSec	0.400%	0.200%	4 Kohms	10 ppm/°C	8 Bits
1809	2.5 µSec	0.200%	0.100%	4 Kohms	10 ppm/°C	9 Bits
1810	3.0 µSec	0.100%	0.050%	4 Kohms	10 ppm/°C	10 Bits
1811	3.5 µSec	0.050%	0.025%	4 Kohms	10 ppm/°C	11 Bits
1812	4.0 µSec	0.025%	0.013%	4 Kohms	10 ppm/°C	12 Bits
1813	8.0 µSec	0.015%	0.010%	4 Kohms	5 ppm/°C	13 Bits
1814	12.0 µSec	0.010%	0.005%	4 Kohms	5 ppm/°C	14 Bits

NOTES: All models and characteristics are available in open-constructed modules. Write for details.

1. Total conversion time from trailing edge of CTC logic level.
2. The conversion error includes all error sources, ±½ LSB and all temperature related errors over the temperature range of 10°C to 40°C for up to 12 bits and 15°C to 35°C for 13 and 14 bit resolution—without adjustments. Should an input range other than that specified at time of purchase be selected, external Gain and Zero Offset adjustment may be necessary.
3. The temperature coefficient includes all gain, zero offset, reference voltage and differential linearity related temperature effects over a range of 0°C to 70°C. For extended operating temperature ranges, the temperature coefficient degrades by a factor of 2 from +70°C to +90°C and from 0°C to -55°C.
4. All specifications are absolute maximums or minimums unless otherwise specified. All models are guaranteed to be monotonic over the operating temperature range of 0°C to 70°C.

2

General Specifications

ANALOG INPUT SIGNAL

Standard Full Scale Ranges (Pin Selectable)

Input Ranges (All Models except 1514, 1614, 1713, 1813 and 1814). See Notes below.

Bipolar	B10	±10 VDC
	B5	± 5 VDC
Unipolar	N10	0 to -10 VDC
	U10	0 to +10 VDC
	U5	0 to + 5 VDC

NOTES:
1. Models 1514, 1614, 1713, 1813 and 1814 have a minimum full-range of 0 to +10,0 to -10 or ±10 VDC
2. 0 to +5.12, 0 to +10.24, 0 to -10.24, ±5.12 and ±10.24 VDC full-range inputs are available on special order.
3. See Range Selection Tables for strapping requirements.

Input Connection	Single Ended (shielded)
Input Impedance	See Specification Tables. 100 megohms available with optional input amplifier (See Ordering Information).
Overvoltage	±30 Volts Max. (±15 Volts with input amplifier).

DIGITAL OUTPUT SIGNALS (TTL/DTL COMPATIBLE)

Parallel Data	8 to 14 binary bits
Logic "1" voltage/current	+2.4 to 5.0 VDC @ 80 μA max.
Logic "0" voltage/current	0 to 0.4 VDC @ -3.2 mA max.
Busy	Logic "1" during conversion.
$\overline{\text{Busy}}$	Complement of Busy.
Data Output Codes	Binary, 2's Complement and Offset Binary (Sign and $\overline{\text{Sign}}$ are brought out)

NOTE: Serial Data Output available on special order.

CONTROL INPUT SIGNALS

Command to Convert (CTC)	200 nSec pulse width min. (TTL/DTL) Conversion initiated on the trailing edge of the CTC pulse. Conversion time measured from trailing edge of CTC pulse (See Table).

ADJUSTMENTS

No internal adjustments.

Pinout is provided for external Gain and Zero Offset potentiometers should the converter be used for output ranges other than that specified on order, or for adjustment due to extended temperature range, etc.

ENCASEMENT SHIELDING

RFI	Protected on six (6) sides
EMI	Protected on five (5) sides.

MECHANICAL

Case material	Hot tin-dipped steel
Repairability	Completely repairable

ENVIRONMENTAL

Temperature	
Operating	0°C to 70°C Standard
Optional	-20°C to 85°C, or -55°C to 90°C
Storage	-55°C to 125°C
Humidity	0 to 99% relative, no condensation
Long Term Stability	0.01% FSR @ 25°C for 12 months
Temperature Coefficient	See Table (Also, see Available Options)

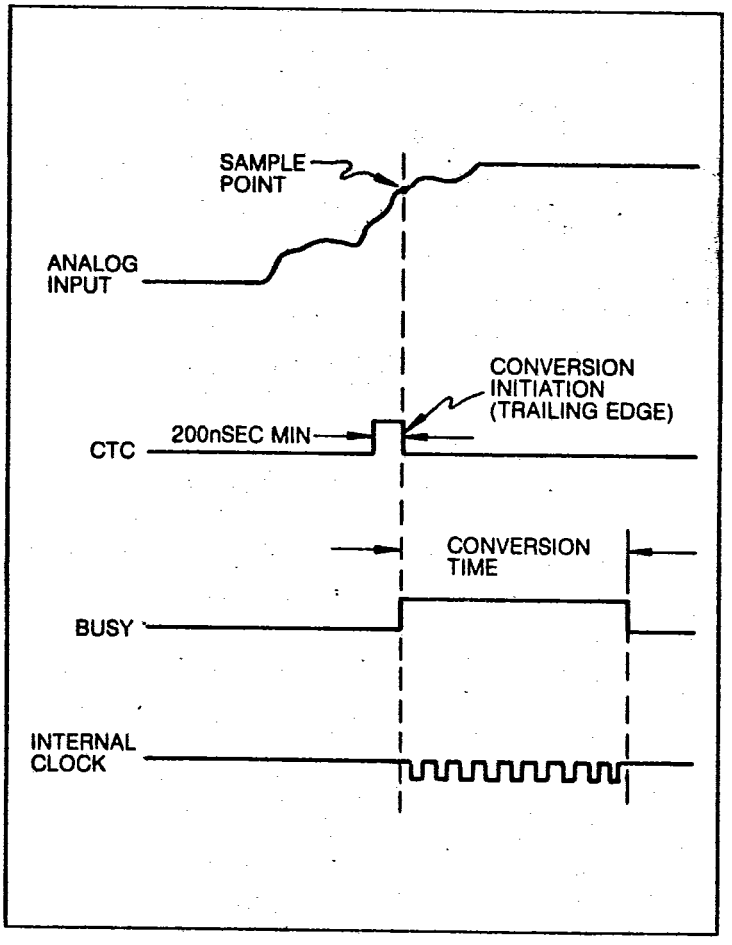
POWER REQUIREMENTS

Voltage and Current (See Note Below)	+15 VDC ±5% @ 60 mA -15 VDC ±5% @ 40 mA +5 VDC ±5% @ 150 mA

NOTE: ±15 VDC ±1% required with no external Gain and Zero Offset Adjustment

Voltage Reference	Internal (Regulated +10 VDC)
Package Configuration	See Physical Dimensions & Pin Connections.

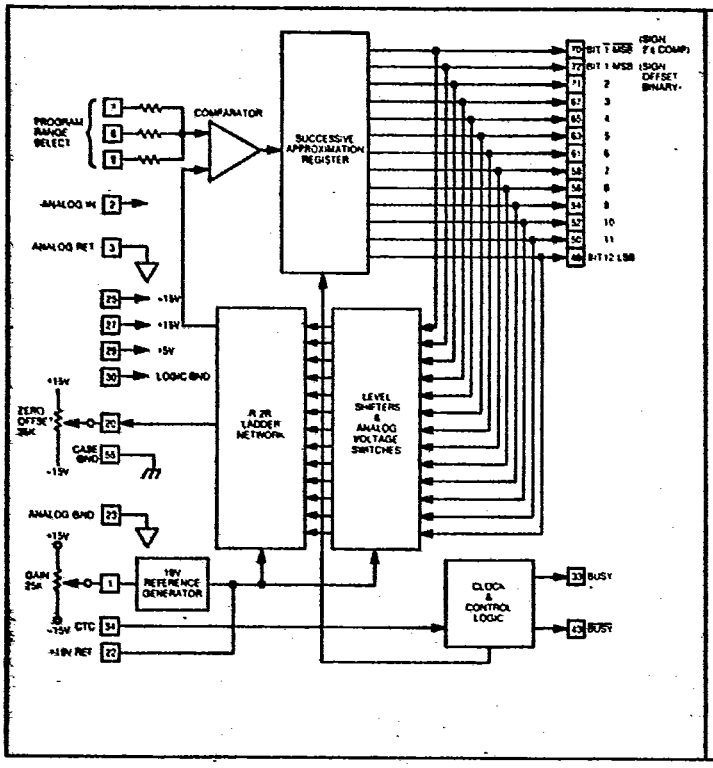
Conversion Timing Diagram



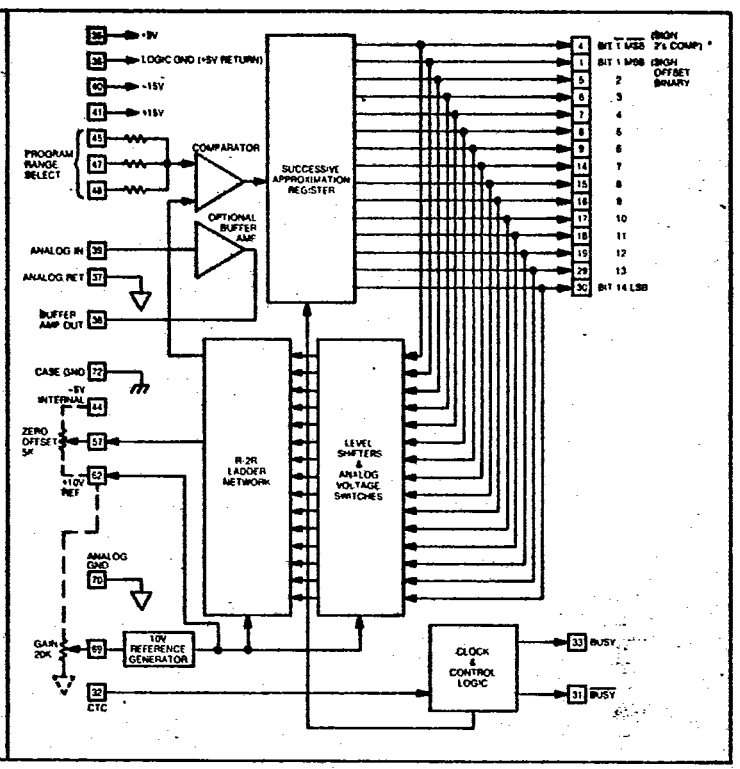
Phoenix Data, Inc.

Application Information

Block Diagram (8 thru 12 Bit Models — All Series)



Block Diagram (13 and 14 Bit Models — All Series)



Programmable Input Range Selection (Pinout jumper connections)

8 thru 12 Bit Models — All Series

BIPOLAR		UNIPOLAR		
B10(±10 VDC)	B5(±5 VDC)	U10(0 to +10 VDC)	N10(0 to -10 VDC)	U5(0 to +5 VDC)
3 to 8	3 to 9	3 to 7	4 to 8	4 to 7
4 to 9	4 to 8	4 to 8	22 to 7	4 to 8
22 to 7	22 to 7	3 to 9	22 to 9	4 to 9

13 and 14 Bit Models — All Series

BIPOLAR		UNIPOLAR		
B10(±10 VDC)	B5(±5 VDC)	U10(0 to +10 VDC)	N10(0 to -10 VDC)	U5(0 to +5 VDC)
47 to 37	48 to 37	45 to 37	47 to 38	45 to 38
48 to 38	47 to 38	47 to 38	45 to 62	47 to 38
45 to 62	45 to 62	48 to 37	48 to 62	48 to 38

Available Options (At additional cost)

1. Full Scale Ranges: 0 to +5.12, 0 to +10.24, 0 to -10.24, ±5.12 and ±10.24 VDC
2. Serial Data Output
3. Temperature Coefficient: 2.5 and 5.0 ppm/°C
4. Temperature: -20°C to 85°C, or -55°C to 90°C
5. Input Buffer Amplifier (Case B, 13 & 14 Bit Models only)
   - A4—Adds 20μSec to conv. time & ½ bit error (13 & 14 bit Models)
   - A5—Adds 1μSec to conv. time & ½ bit error (13 bit Models)
   - A6—Adds 2μSec to conv. time & ½ bit error (14 bit Models)
   - A7—Adds 20μSec to conv. time & ½ bit error (13 & 14 bit Models) FET Input Amplifier
   - A8—Adds 1μSec to conv. time & ½ bit error (13 bit Models) FET Input Amplifier
   - A9—Adds 2μSec to conv. time & ½ bit error (14 bit Models) FET Input Amplifier
6. Mil. Spec & high reliability, hermetically sealed modules
7. All Models available mounted on adaptor card with 44-pin card edge connector

Installation

POWER CONNECTIONS
If the ADC is to be remotely located three (3) feet or more from its external power source, each power supply voltage lead should be twisted with its respective ground return. Also, should the ADC be located in a rack or chassis with other equipment, all operating from a common power supply, then careful attention to system grounding and power distribution rules should be considered to prevent ground loops and cross-talk between system components.

DIGITAL INPUT SIGNALS
All digital input control signals drive standard TTL compatible integrated circuits, with each input representing one TTL unit load. All normal precautions associated with TTL input logic should apply.

DIGITAL OUTPUT SIGNALS
All digital output signals are derived from TTL compatible integrated circuits, with each output capable of driving six (6) TTL unit loads.

ANALOG INPUT
To minimize noise, it is recommended that a twisted-pair, shielded cable be used to connect the analog input and analog return lines of the ADC to source device. The shield should be connected to the analog return line at one end only — preferably at the source end.

GROUND CONNECTIONS
The common (ground) return for the ±15 VDC supplies and the +5 VDC supply are not connected internally. It is recommended that this connection be made at the ADC pinout. If the connection is not made at the ADC pinout, caution should be taken to limit the voltage difference between the ADC power supply ground return pins to ±0.25 VDC maximum, including DC offset and peak noise.

Warning Notes

POWER SUPPLY OVERVOLTAGE
Externally supplied power voltages must not exceed specified limits for proper ADC operation. Power supply turn-on/turn-off surging must be suppressed to prevent damage to the ADC circuit. Permanent damage may occur if transients greater than ±18 VDC or +7 VDC are present on the ±15 VDC and +5 VDC supply lines respectively.

A short circuit of any input/output connection to any power supply voltage can cause permanent damage to the ADC. Also, a short circuit of any input/output connection to ground will not damage the ADC, except for the reference voltage output.

External Gain and Zero Offset Adjustment

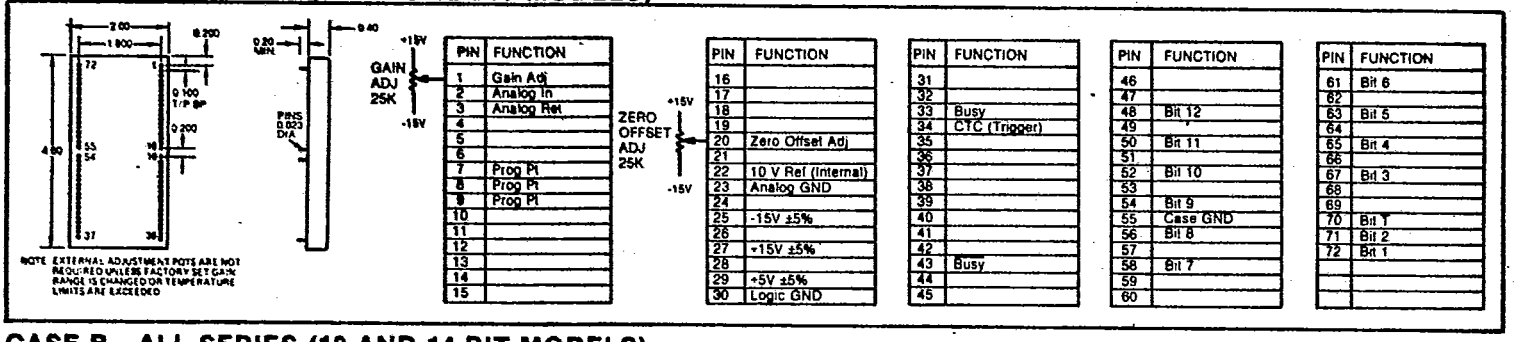
EXTERNAL ZERO ADJUST
Adjust external zero potentiometer for zero code output with 0.0 VDC input.

EXTERNAL GAIN ADJUST
Adjust the external gain potentiometer such that the output code from -F.S. to +F.S. is equal to the specified full-range, less *one* LSB. For bipolar units, the positive F.S. code should be equal to $\left(2^{\frac{[\text{No. of Bits}]}{2}}-1\right)$ bit weight or (½ full range minus one LSB); and, the negative F.S. code should be equal to $\left(2^{\frac{[\text{No. of Bits}]}{2}}\right)$ bit weight or (½ full range).

F.S. = Full Scale

Physical Dimensions & Pin Connections

CASE A - ALL SERIES (8 THRU 12 BIT MODELS)



PIN	FUNCTION
1	Gain Adj
2	Analog In
3	Analog Ret
4	
5	
6	
7	Prog Pt
8	Prog Pt
9	Prog Pt
10	
11	
12	
13	
14	
15	

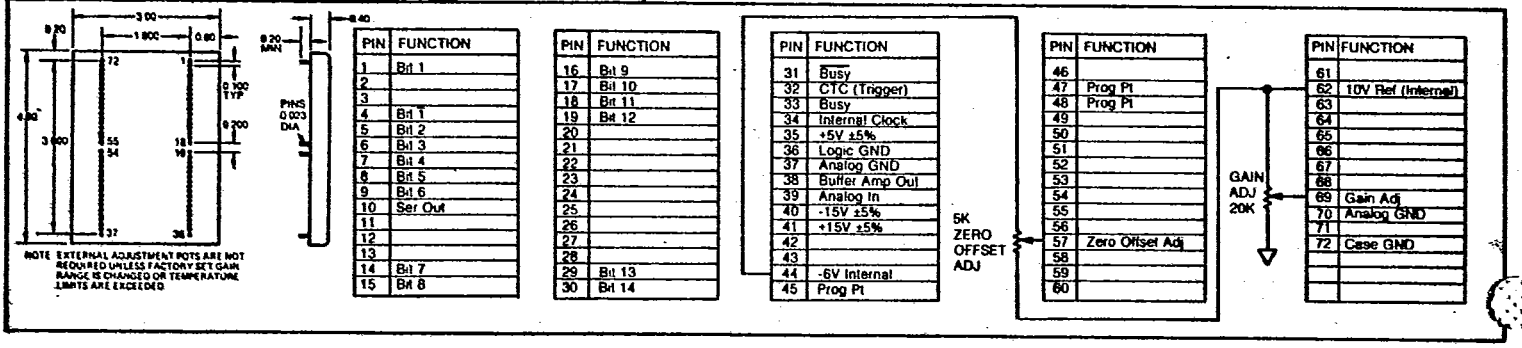
PIN	FUNCTION
16	
17	
18	
19	
20	Zero Offset Adj
21	
22	10 V Ref (Internal)
23	Analog GND
24	
25	-15V ±5%
26	
27	+15V ±5%
28	
29	+5V ±5%
30	Logic GND

PIN	FUNCTION
31	
32	
33	Busy
34	CTC (Trigger)
35	
36	
37	
38	
39	
40	
41	
42	
43	Busy
44	
45	

PIN	FUNCTION
46	
47	
48	Bit 12
49	
50	Bit 11
51	
52	Bit 10
53	
54	Bit 9
55	Case GND
56	Bit 8
57	
58	Bit 7
59	
60	

PIN	FUNCTION
61	Bit 6
62	
63	Bit 5
64	
65	Bit 4
66	
67	Bit 3
68	
69	
70	Bit T
71	Bit 2
72	Bit 1

CASE B - ALL SERIES (13 AND 14 BIT MODELS)



PIN	FUNCTION
1	Bit 1
2	
3	
4	Bit 1
5	Bit 2
6	Bit 3
7	Bit 4
8	Bit 5
9	Bit 6
10	Ser Out
11	
12	
13	
14	Bit 7
15	Bit 8

PIN	FUNCTION
16	Bit 9
17	Bit 10
18	Bit 11
19	Bit 12
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	Bit 13
30	Bit 14

PIN	FUNCTION
31	Busy
32	CTC (Trigger)
33	Busy
34	Internal Clock
35	+5V ±5%
36	Logic GND
37	Analog GND
38	Buffer Amp Out
39	Analog In
40	-15V ±5%
41	+15V ±5%
42	
43	
44	-6V Internal
45	Prog Pt

PIN	FUNCTION
46	
47	Prog Pt
48	Prog Pt
49	
50	
51	
52	
53	
54	
55	
56	
57	Zero Offset Adj
58	
59	
60	

PIN	FUNCTION
61	
62	10V Ref (Internal)
63	
64	
65	
66	
67	
68	
69	Gain Adj
70	Analog GND
71	
72	Case GND

Ordering Information

XXXX X XXX XX XX XX

Model Number

B = Bipolar Input
U = Unipolar Input (+)
N = Unipolar Input (-)

005 = 0 to +5 ±5 VDC
010 = 0 to +10 0 to -10 ±10 VDC
A05 = 0 to +5 12, ±5 12 VDC
A10 = 0 to +10 24, 0 to -10 24, ±10.24 VDC

Input Buffer Amp (Case B, 13 & 14 bit Models only)

A4, A5, A6, A7, A8 or A9
(See Option Table)

ST = Std. T.C.
50 = 5.0ppm/°C
25 = 2.5ppm/°C

ST = Std. Temp. Range
MT = -20°C to 85°C
HT = -55°C to 90°C

Warranty

Phoenix Data, Inc. warrants its products to be free from defects in material and workmanship, under normal use and service, for a period of 90 days from date of original shipment. Warranty obligations shall be limited to replacing or repairing, at our option, any product returned, transportation charges prepaid, and found to be defective within the warranty period.

For additional information, contact your Phoenix Data representative, or:

Phoenix Data, Inc.
3384 West Osborn Road, Phoenix, Arizona 85017, Phone 602/278-8528 TWX 910-951-1364

Representative

LITHO USA, EADC-1001-1076